# VHF/UHF Tuner IC for Multi-Standard Digital TV

Preliminary Technical Data

# ADMTV803

## FEATURES

- Single-chip RF tuner IC for Multi-Standard Digital TV
- Applications in VHF and UHF
  - VHF (54 MHz to 245 MHz)
  - UHF (470 MHz to 862 MHz)
- Zero-IF architecture
- Low noise figure 3.5 dB
- Typical AGC dynamic range: −102 dBm to +10 dBm
- Low power consumption in continuous mode
  - VHF: 98 mW
  - UHF: 98 mW
- On-chip features include
  - Fast switching fractional-N PLL
  - Low phase noise and wide frequency range VCO
  - PLL loop filter
  - Bandwidth-adjustable low-pass filter
  - Reference clock output for demodulators
- Integrated baseband PGA for direct connection to digital demodulators
- Noise/linearity optimization through internal RFAGC loop
- Adjustable take-over point
- $I^2C$ serial bus interface
- Small 24-lead lead frame chip scale package (LFCSP)
  (4 mm × 4 mm)
- Minimal external components
  - 6 ea for UHF only
  - 9 ea for dual-band

## APPLICATIONS

- CMMB (UHF band) /DTMB/ DVB-H/ DVB-T/ DAB/ T-DMB/ ATSC-M/H/ ISDB-T (full-seg, 3-seg and 1-seg) mobile and portable TV receivers
- VHF/UHF mobile and portable TV receivers

## FUNCTIONAL BLOCK DIAGRAM

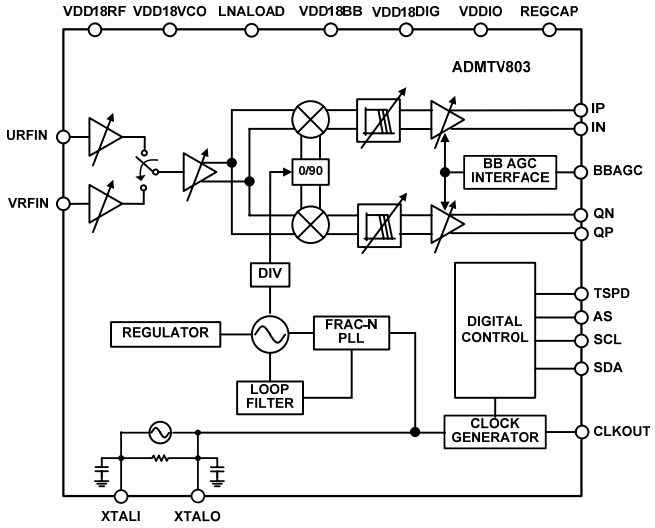


*Figure 1.*

## GENERAL DESCRIPTION

The ADMTV803 is a highly integrated CMOS zero-IF conversion tuner IC for multi-standard digital TV such as CMMB (UHF band), DTMB, DVB-H, DVB-T, DAB, T-DMB, ATSC-M/H and ISDB-T (full-seg, 3-seg and 1-seg). It supports dual RF input bands, VHF and UHF. The building blocks include LNA, RFPGA, I/Q down- conversion mixer, bandwidth adjustable low-pass filter, baseband PGA, and fractional-N frequency synthesizer with fully integrated VCO and PLL loop filter. The on-chip low phase noise VCO, along with the high resolution fractional-N frequency synthesizer makes in-band phase noise low enough for mobile TV applications.

The ADMTV803 consumes less than 9.8 mW for DVB-H mode at 10 % duty cycle. By using very small package size (LFCSP), the ADMTV803 is the best solution for mobile TV application especially for mobile phones, notebook PCs, PDAs, etc. where low power consumption is required critically.

Applications for the ADMTV803 include CMMB (UHF band), DTMB, DVB-H, DVB-T, DAB, T-DMB, ATSC-M/H and ISDB-T (full-seg, 3-seg and 1-seg).

**Rev. PrB**



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## REVISION HISTORY

**03/09/2009—Revision PrB: Preliminary**

# SPECIFICATIONS

## DC ELECTRICAL CHARACTERISTICS

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OPERATING CONDITIONS | | | | | |
| 1.8 V Supply Voltage (VDD18RF, VDD18VCO, LNALOAD, VDD18BB, VDD18DIG) | $V_{DD18}$ | 1.7 | 1.8 | 1.9 | V |
| I/O Supply Voltage (VDDIO) | $V_{DDIO}$ | 1.7 | 2.8 | 3.6 | V |
| BBAGC Input Voltage | $V_{BBAGC}$ | 0 | | 3.6 | V |
| BBAGC Input Current | $I_{BBAGC}$ | -10 | | 10 | µA |
| DIGITAL INPUT/OUTPUT PINS (TSPD, AS, SCL, SDA, CLKOUT) | | | | | |
| Maximum Low Input Voltage | $V_{IL}$ | | | $0.3 \times V_{DDIO}$ | V |
| Minimum High Input Voltage | $V_{IH}$ | $0.7 \times V_{DDIO}$ | | | V |
| Maximum Low Output Voltage | $V_{OL}$ | | | $0.4 \times V_{DDIO}$ | V |
| Minimum High Output Voltage | $V_{OH}$ | $V_{DDIO} - 0.4$ | | | V |
| High Level Input Current ($V_{IN} = V_{DDIO}$) | $I_{IH}$ | -10 | | 10 | µA |
| Low Level Input Current ($V_{IN}$ = GND) | $I_{IL}$ | -10 | | 10 | µA |
| VHF POWER CONSUMPTION | | | | | |
| 1.8 V Analog Current Consumption | $I_{DD18AVHF}$ | | 50 | | mA |
| 1.8 V Digital Current Consumption | $I_{DD18DVHF}$ | | 4.5 | | mA |
| I/O Digital Current Consumption | $I_{DDIOVHF}$ | | 3 | | µA |
| Power-Down Current Consumption | $I_{PDVHF}$ | | TBD | | µA |
| Total Power Consumption | $P_{VHF}$ | | 98 | | mW |
| UHF POWER CONSUMPTION | | | | | |
| 1.8 V Analog Current Consumption | $I_{DD18AUHF}$ | | 50 | | mA |
| 1.8 V Digital Current Consumption | $I_{DD18DUHF}$ | | 4.5 | | mA |
| I/O Digital Current Consumption | $I_{DDIOUHF}$ | | 3 | | µA |
| Power-Down Current Consumption | $I_{PDUHF}$ | | TBD | | µA |
| Total Power Consumption | $P_{UHF}$ | | 98 | | mW |

## AC ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C, $V_{DD12}$ = 1.2 V, $V_{DDIO}$ = 2.8 V, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REFERENCE CRYSTAL OR CLOCK INPUT FREQUENCY | $f_{CLK}$ | 13 | | 40 | MHz |
| VHF CHARACTERISTICS | | | | | |
| RF Frequency Range | $f_{VHF}$ | 54 | | 245 | MHz |
| RF Input Impedance | $Z_{IN}$ | | 50 | | Ω |
| Input VSWR | VSWR | | 2:1 | 3:1 | |
| Typical AGC Dynamic Range | $P_{IN}$ | -102 | | 10 | dBm |
| Noise Figure @ Maximum Gain | NF | | 3.5 | | dB |
| In-Band Two-Tone IMD3 (U/D)[1] | $IMD3_{IN}$ | | 70 | | dBc |
| Out-of-Band IIP3[2] | $IIP3_{OUT}$ | | -7 | | dBm |
| 3 dB Cutoff Frequency[3] | $f_{3dB}$ | 0.29 | | 4 | MHz |
| Stop Band Attenuation[4] | SBA | | -65 | | dBc |
| LO Phase Noise (SSB @ 100 kHz Offset) | $PN_{100k}$ | | -107 | | dBc/Hz |
| Baseband Output Amplitude $V_{pp}$, Single | $V_{OUTAC}$ | | 500 | 700 | mV |
| Baseband Output Pins (QP, QN, IN, IP) | | | | | |
| Minimum Load Resistance, Differential | $R_{L\ MIN}$ | 2 | | | kΩ |
| Maximum Load Capacitance, Differential | $C_{L\ MAX}$ | | | 20 | pF |
| Output DC Voltage | $V_{OUTDC}$ | | 0.9 | | V |
| UHF CHARACTERISTICS | | | | | |
| RF Frequency Range | $f_{UHF}$ | 470 | | 862 | MHz |
| RF Input Impedance | $Z_{IN}$ | | 50 | | Ω |
| Input VSWR | VSWR | | 2:1 | 3:1 | |
| Typical AGC Dynamic Range | $P_{IN}$ | -102 | | 10 | dBm |
| Noise Figure @ Maximum Gain | NF | | 3.5 | | dB |
| In-Band Two-Tone IMD3 (U/D)[1] | $IMD3_{IN}$ | | 63 | | dBc |
| Out-of-Band IIP3[2] | $IIP3_{OUT}$ | | -8 | | dBm |
| 3 dB Cutoff Frequency[3] | $f_{3dB}$ | 0.29 | | 4 | MHz |
| Stop Band Attenuation[4] | SBA | | -65 | | dBc |
| LO Phase Noise (SSB @ 100 kHz Offset) | $PN_{100k}$ | | -97 | | dBc/Hz |
| Baseband Output Amplitude $V_{pp}$, Single | $V_{OUTAC}$ | | 500 | 700 | mV |
| BB Output Pins (QP, QN, IN, IP) | | | | | |
| Minimum Load Resistance, Differential | $R_{L\ MIN}$ | 2 | | | kΩ |
| Maximum Load Capacitance, Differential | $C_{L\ MAX}$ | | | 20 | pF |
| Output DC Voltage | $V_{OUTDC}$ | | 0.9 | | V |

[1] For RF input power, PIN < -30dBm, f1-f2=500kHz frequency offset

[2] For RF input power, PIN = -80dBm, two-tone interferer power = -35dBm, f1 = 13.25 MHz frequency offset, f2 = 29.25 MHz frequency offset. RFAGC: closed-loop gain control, BBAGC: external gain control.

[3] Programmable

| MULTI-BAND CHARACTERISTICS | CMMB | DTMB, DVB-H, DVB-T | DAB, T-DMB | ATSC-M/H | ISDB-T full-seg | ISDB-T 3-seg | ISDB-T1-seg |
|---|---|---|---|---|---|---|---|
| Signal Bandwidth (MHz) | 2, 8 | 5, 6, 7, 8 | 1.536 | 6 | 6 | 1.29 | 0.43 |
| 3 dB Cutoff Frequency (MHz) | 1, 4 | 2.5, 3, 3.5, 4 | 0.768 | 3 | 3 | 0.645 | 0.29 |

[4] For 4.87 MHz offset @ 4MHz LPF offset

## POWER AND DIGITAL TIMING CHARACTERISTICS

**Table 3.**

| Parameter | Symbol[1] | Min | Unit |
|---|---|---|---|
| TSPD Setup Margin | A | Don't Care | µs |
| Power-Up Setup Margin for $V_{DD18}$ | B | Don't Care | µs |
| Power-Up Setup Margin for $V_{DDIO}$ | C | Don't Care | µs |
| Setup Time for $I^2C$ Interface | D | 10 | µs |

[1] see figure 2.

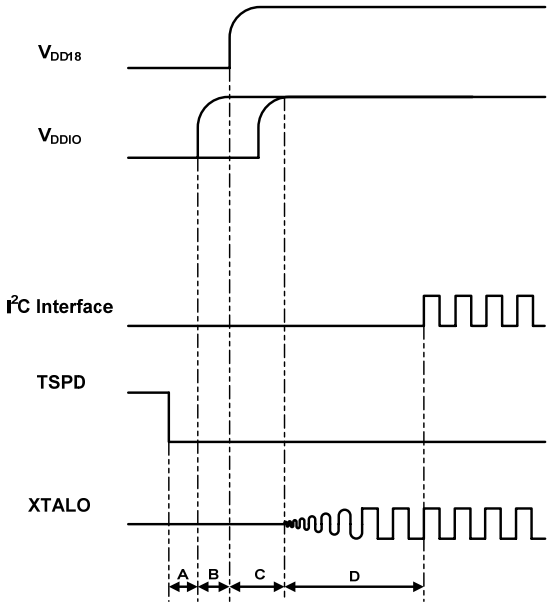



*Figure 2 . Power and Digital Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| 1.8 V Supply Voltage ($V_{DD18}$) | −0.5 V to +2.1 V |
| I/O Supply Voltage ($V_{DDIO}$) | −0.5 V to + 4.0 V |
| Analog Input Voltage | −0.5 V to $V_{DD18}$ + 0.3 V |
| Digital Input Voltage | −0.5 V to $V_{DDIO}$ + 0.5 V |
| Analog Output Voltage | −0.5 V to $V_{DD18}$ + 0.3 V |
| Digital Output Voltage | −0.5 V to $V_{DDIO}$ + 0.5 V |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

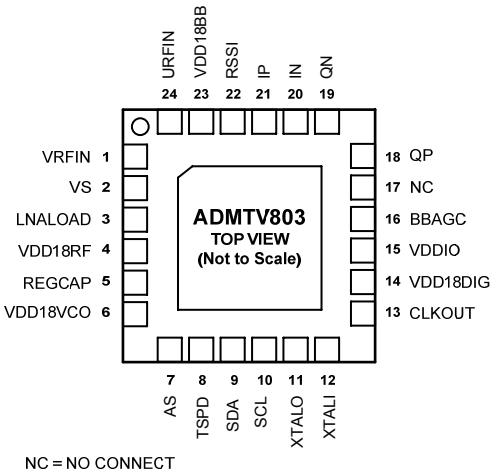



*Figure 3. Pin Configuration [LFCSP]*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | I/O Type[1] | Description |
|---|---|---|---|
| 1 | VRFIN | AI | VHF RF Input. |
| 2 | VS | AO | VHF LNA Source. A 3.3 nH inductor should be connected as close as possible between this pin and GND. |
| 3 | LNALOAD | P | RF Power (1.8 V). This pin should be decoupled with a 1 nF capacitor. |
| 4 | VDD18RF | P | RF Power (1.8 V). This pin should be decoupled with a 1 nF capacitor. |
| 5 | REGCAP | P | Regulator output decoupling capacitor. This pin should be decoupled with a 470 nF capacitor. |
| 6 | VDD18VCO | P | VCO Power (1.8 V). This pin should be decoupled with a 1 nF capacitor. |
| 7 | AS | DI | Address Selection. The $I^2C$ address can be determined by the AS pin.<br>If AS is connected to GND, read mode address = 0xC3, write mode address = 0xC2.<br>If AS is connected to VDDIO, read mode address = 0xC5, write mode address = 0xC4. |
| 8 | TSPD | DI | Time-Slicing Power-Down. Apply 0 V to this pin for normal operation. Apply VDDIO for time-slicing power-down. |
| 9 | SDA | DB | $I^2C$ Data. Bidirectional pin. 10kΩ pull up resistor is embedded on chip. |
| 10 | SCL | DI | $I^2C$ Clock. 10kΩ pull up resistor is embedded on chip. |
| 11 | XTALO | AO | Crystal Oscillator Output. |
| 12 | XTALI | AI | Crystal Oscillator Input. |
| 13 | CLKOUT | AO | Clock Output. |
| 14 | VDD18DIG | P | Digital Power (1.8 V). |
| 15 | VDDIO | P | Wide Range I/O Power (1.8 V to 3.3 V). |
| 16 | BBAGC | AI | BBAGC Input (0 V to 3.3 V). |
| 17 | NC | | No connection. |
| 18 | QP | AO | Quadrature-Phase Positive Output. |
| 19 | QN | AO | Quadrature-Phase Negative Output. |
| 20 | IN | AO | In-Phase Negative Output. |
| 21 | IP | AO | In-Phase Positive Output. |
| 22 | RSSI | AO | RSSI Output voltage for Adjacent Channels. A 33nF capacitor should be connected as close as possible between this pin and GND. |
| 23 | VDD18BB | P | Baseband Block Power (1.8 V). This pin should be decoupled with a 100 nF capacitor. |
| 24 | URFIN | AI | UHF RF Input. |

[1] AI = Analog input, AO = Analog output, DI = Digital input, DO = Digital output, DB = Digital bidirectional, P = Power

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $V_{DD18}$ = 1.8 V, $V_{DDIO}$ = 3.3 V, unless otherwise noted.

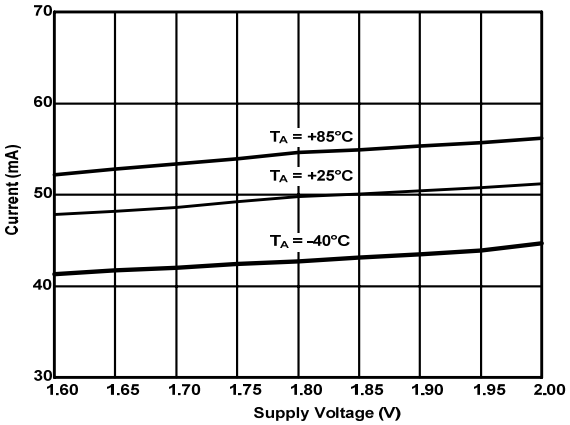



*Figure 4. UHF Receiver Mode Current vs. Supply Voltage*

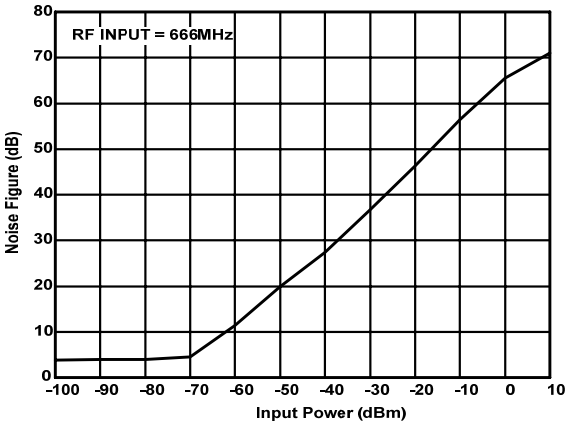



*Figure 7. UHF Noise Figure vs. Input Power*

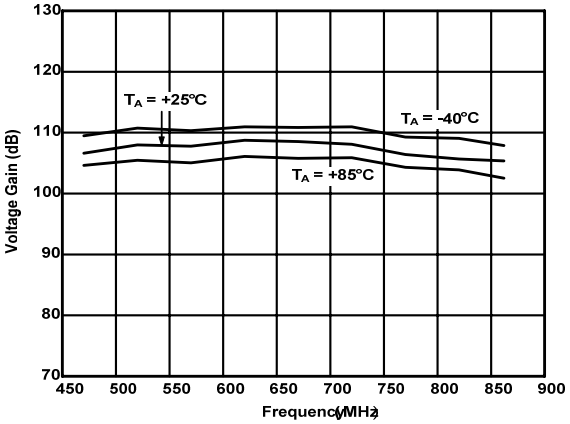



*Figure 5. UHF Maximum Voltage Gain vs. Frequency*

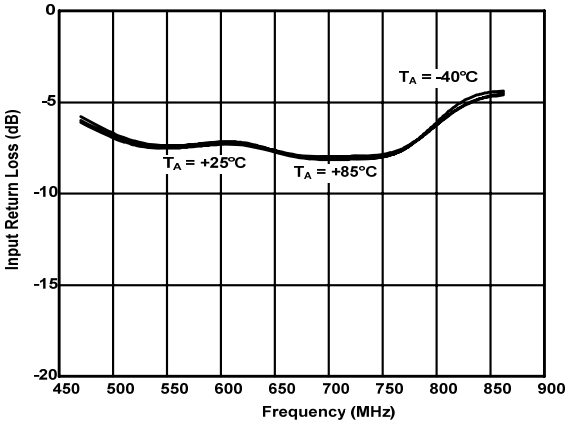



*Figure 8. UHF Input Return Loss (S11) vs. Frequency (High LNA Gain Mode)*

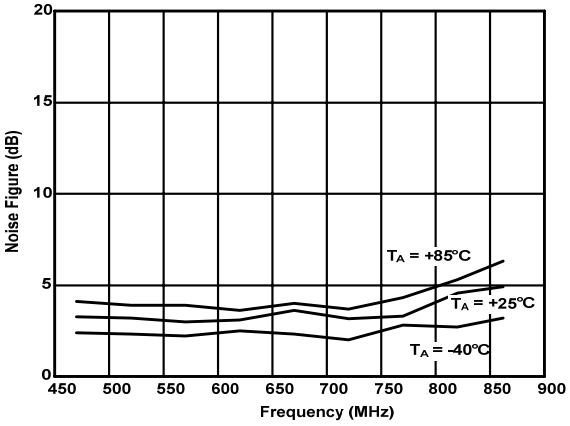



*Figure 6. UHF Noise Figure vs. Frequency*

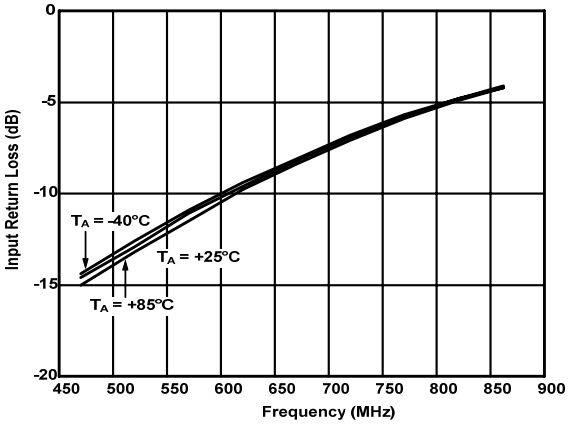



*Figure 9. UHF Input Return Loss (S11) vs. Frequency (Very Low LNA Gain Mode)*

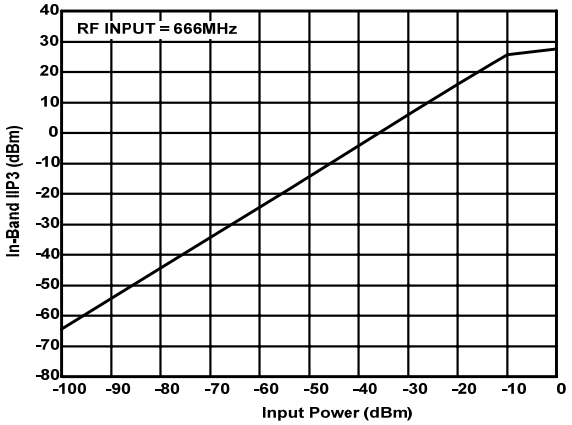



Figure 10. UHF In-Band IIP3 vs. Input Power

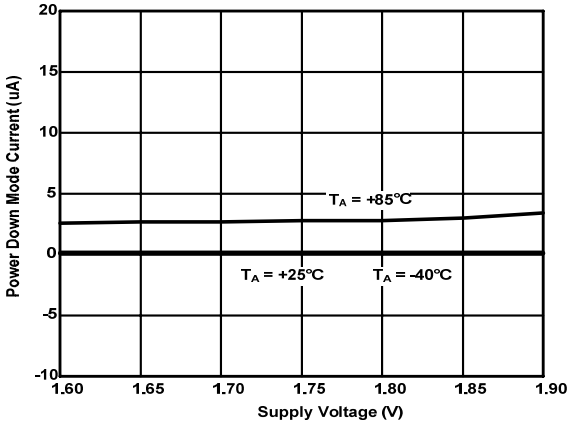



Figure 13. UHF Power-Down Mode Current vs. Supply Voltage

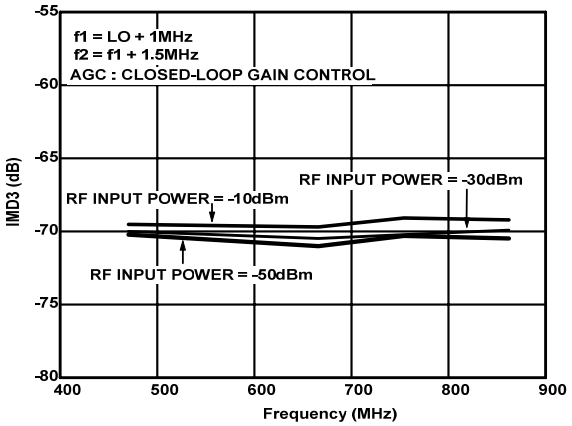



Figure 11. UHF In-Band IMD3 vs. Frequency

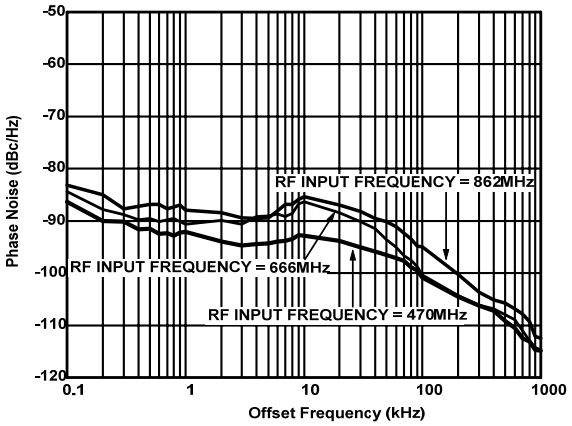



Figure 14. UHF Phase Noise vs. Offset Frequency

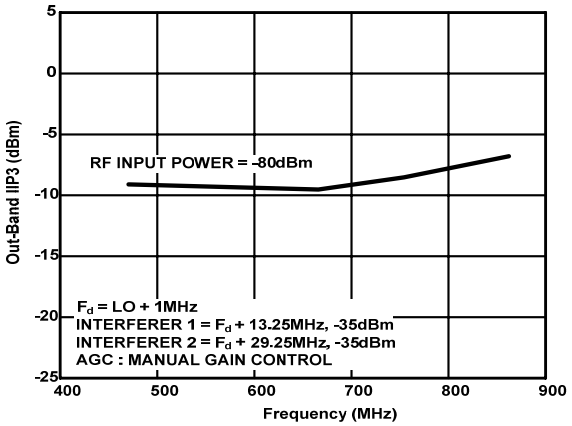



Figure 12. UHF Out-of-Band IIP3 vs. Frequency

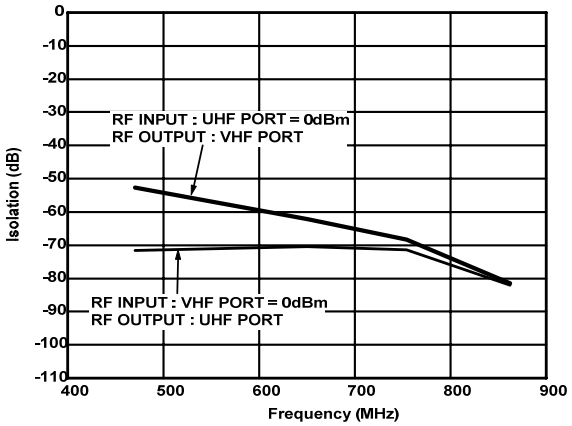



Figure 15. Port-to-Port Isolation

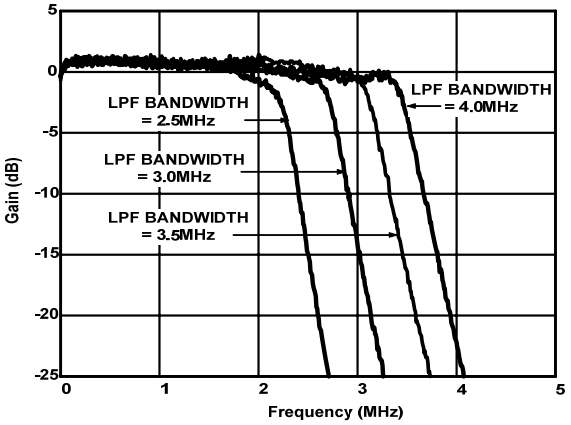



*Figure 16. UHF Tunable Low-Pass Filter Response*

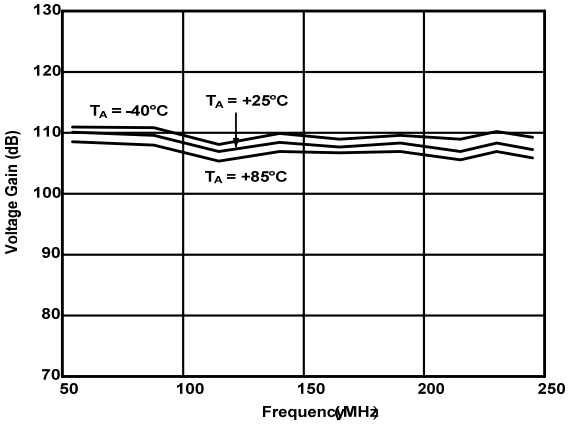



*Figure 19. VHF Maximum Voltage Gain vs. Frequency*

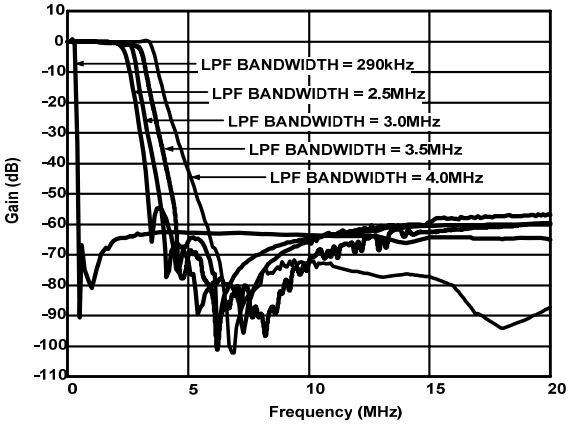



*Figure 17. UHF Tunable Low-Pass Filter Attenuation*

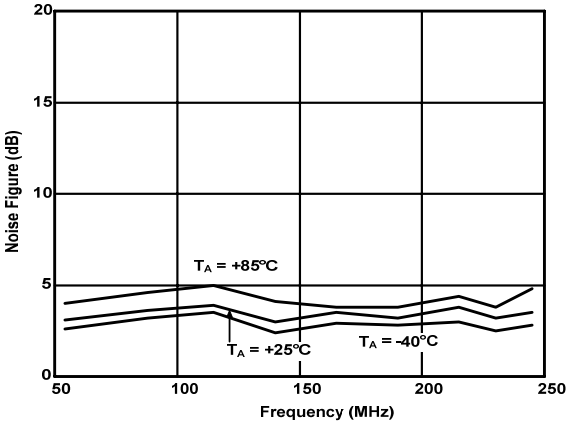



*Figure 20. VHF Noise Figure vs. Frequency*

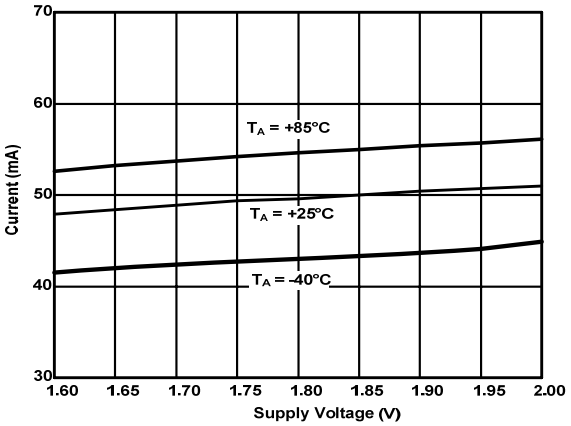



*Figure 18. VHF Receiver Mode Current vs. Supply Voltage*

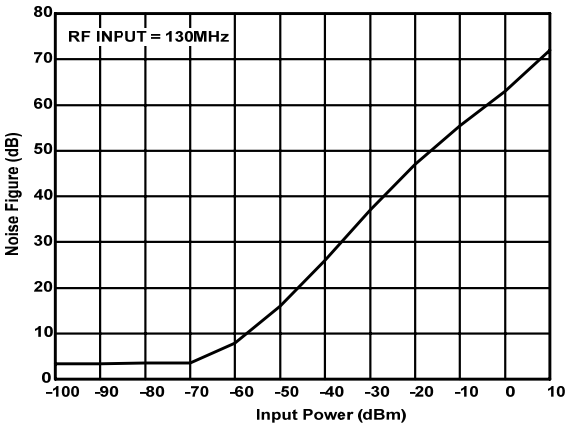



*Figure 21. VHF Noise Figure vs. Input Power*

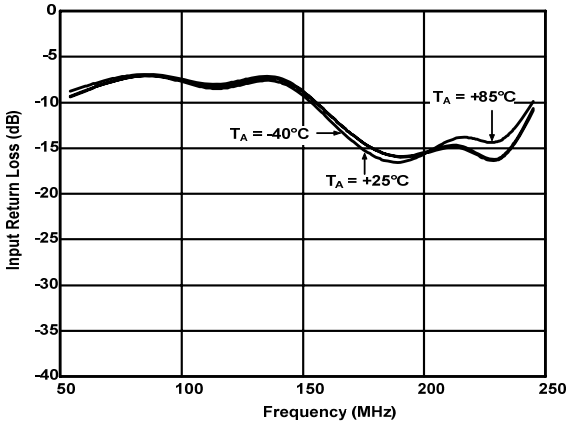



*Figure 22. VHF Input Return Loss (S11) vs. Frequency*

*(High LNA Gain Mode)*

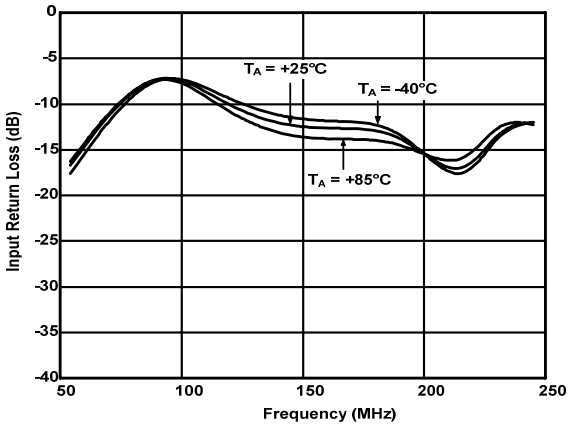



*Figure 23. VHF Input Return Loss (S11) vs. Frequency*

*(Very Low LNA Gain Mode)*

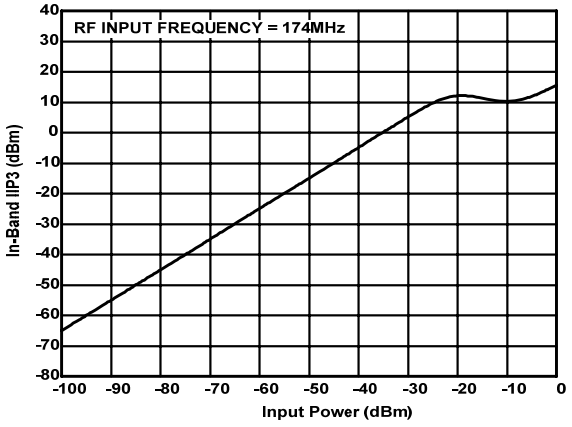



*Figure 24. VHF In-Band IIP3 vs. Input Power*

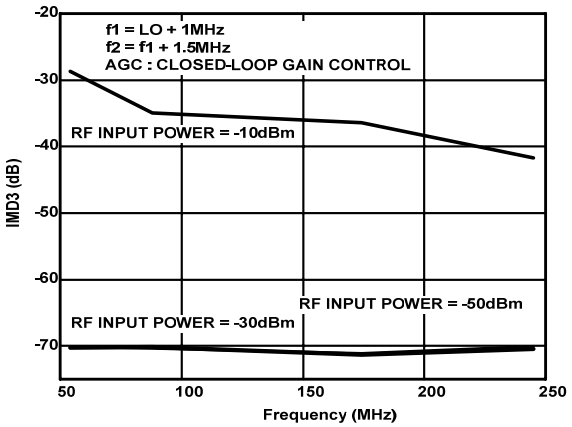



*Figure 25. VHF In-Band IMD3 vs. Frequency*

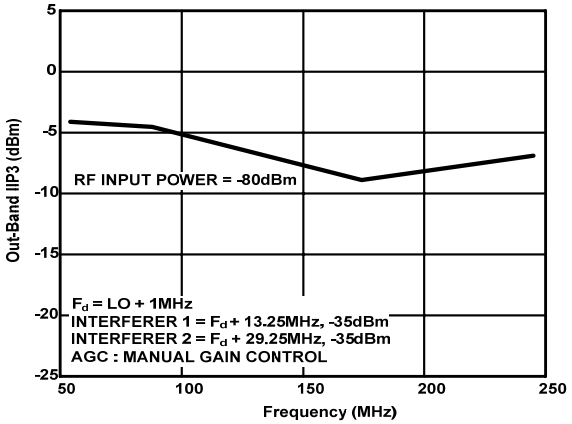



*Figure 26. VHF Out-of-Band IIP3 vs. Frequency*

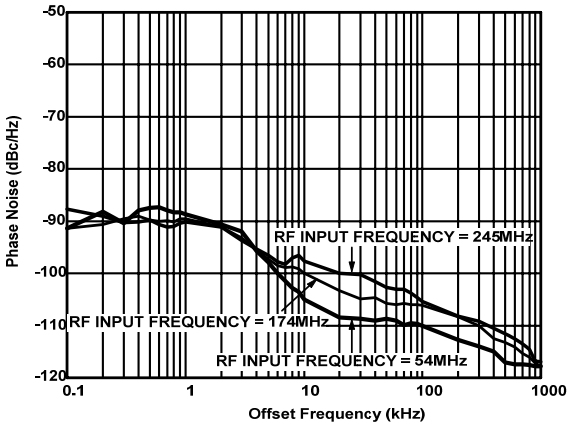



*Figure 27. VHF Phase Noise vs. Offset Frequency*

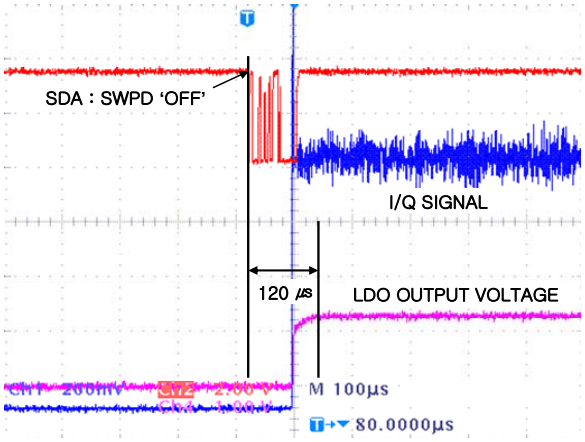



*Figure 28. Software Power-On Timing*

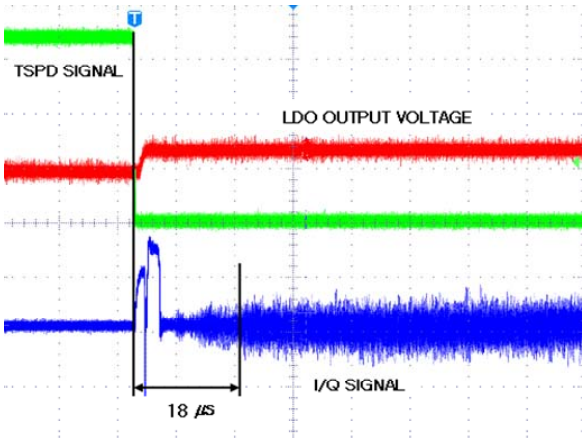



*Figure 29. Time-Slicing Power-On Timing*

# TERMINOLOGY

**Input Third-Order Intercept (IIP3)**
A figure of merit used to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its third-order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f1 and f2) are injected into a nonlinear system exhibiting third-order nonlinearities, producing IMD components at (2 × f1) − f2 and (2 × f2) − f1. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third-order IMD component when plotted in decibels.

**Intermodulation Distortion (IMD)**
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa, nfb, where m and n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to zero.
For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

**Noise Figure (NF)**
Noise Figure is a measure of how much the SNR degrades as the signal passes through a system.

$$Noise\ Figure = \frac{SNR_{in}}{SNR_{out}}$$

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the average signal power to average noise power, excluding harmonics and DC. The value for SNR expresses in decibels.

**Voltage Standing-Wave Ratio (VSWR)**
The ratio of the maximum effective voltage to the minimum effective voltage measured along the length of a mismatched radio frequency transmission line.

# THEORY OF OPERATION

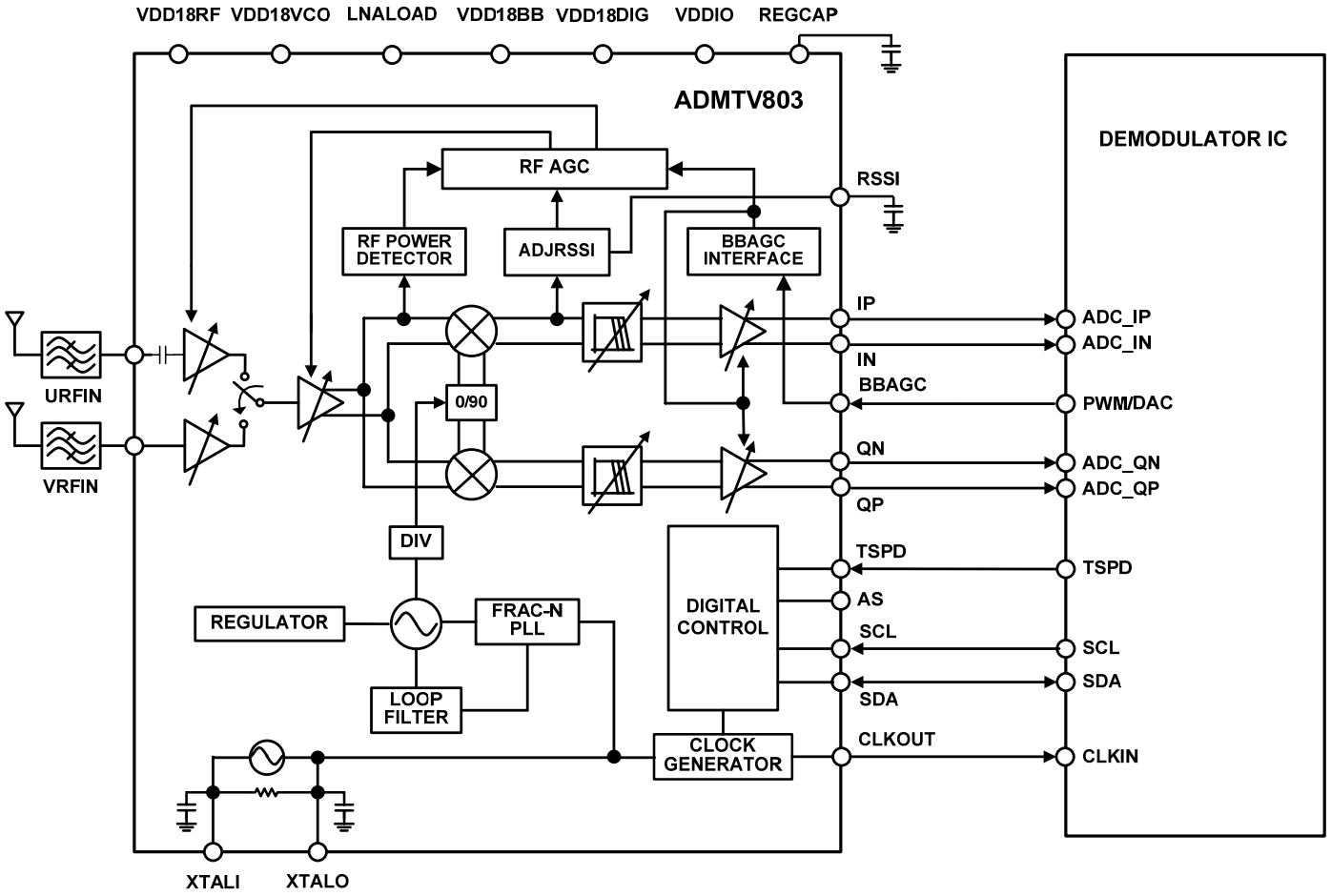



*Figure 30. ADMTV803 Interface*

## LOW NOISE AMPLIFIER (LNA)

ADMTV803 LNA consists of two LNA, and each LNA supports VHF (40~245MHz) band and UHF (470~862MHz) band. The LNA has 4 gain modes, which are 18 dB, 7 dB, -3 dB and -21 dB typically. The LNA gain state can be read from the LNAGAIN register. When LNAGAIN<1:0>=0x3, the gain is in high gain state, LNAGAIN<1:0>=0x2, the gain is in middle gain state, LNAGAIN<1:0>=0x1, the gain is in low gain state, and LNAGAIN<1:0>=0x0, the gain is in very low gain state.

## RF PROGRAMMABLE GAIN AMPLIFIER (PGA)

The RFPGA has a dynamic gain range of 36 dB. RFPGA gain is controlled by digital gain code, which can be read from the RFAGC register. RFAGC register ranges from 0x00 (minimum gain) to 0x5F (maximum gain). The gain step is 0.5 dB.

## I/Q DOWNCONVERTER

The I/Q downconversion mixer amplifies incoming RF signals from the RFPGA output and converts the signals to baseband.

## LOCAL OSCILLATOR

### *Voltage Controlled Oscillator (VCO)*

The ADMTV803 includes an on-chip VCO, which eliminates the need for an external LC tank. This internal VCO uses only 1.8 V and covers the VHF band (54 MHz to 245 MHz) and the UHF band (470 MHz to 862 MHz). Along with the fractional-N PLL, this low phase noise VCO guarantees sufficient performance for mobile reception of worldwide mobile TV.

### *Phase Locked Loop (PLL)*

The PLL synthesizer includes integrated 20-bit fractional-N PLL and integrated loop filter. Integrated loop filter eliminates extra external passive components. In addition to the integrated VCO, the ADMTV803 local oscillator consists of a Σ-Δ fractional-N PLL

frequency synthesizer. The fractional-N type architecture with a high performance 20-bit Σ-Δ modulator obtains high resolution and fast switching times, as well as good phase noise.

To compensate variable VCO gain, control bits of CP_COMP<4:0> are available. Unlike integer-N type synthesizers used in other silicon tuners, Σ-Δ modulated frequency synthesizers provide the following features:

- Fast switching time.
- Ultra high frequency resolution.
- Good phase noise due to its wide bandwidth.

Using a 30.4 MHz crystal oscillator with a 20-bit Σ-Δ modulated fractional-N PLL exhibits a very fine frequency resolution of 29 Hz. The PLL can compensate the frequency offset induced by such factors as the frequency error of reference crystal and the temperature drift of a crystal.

The local oscillator frequency, $f_{LO}$, is calculated as the following equations:

$$f_{PLL} = \frac{f_{crytal}}{PLLR} \cdot \left( PLLN + \frac{PLLF}{2^{20}} \right)$$

$$f_{LO} = \frac{f_{PLL}}{PLLS}$$

Where:
*PLLN* is the integer divide value selected by the PLLN register.
*PLLF* is the fractional divide value selected by the PLLF register.

*PLLR* is the reference crystal frequency divide ratio selected by PLLR register.
*PLLS* is selected by the VCOLOADBAND<1:0> register value and VCOBAND<1:0> register and frequency range decides VCOLOADBAND<1:0> register value (see the PLL Setting section for more information).

## BASEBAND PROGRAMMABLE GAIN LOW-PASS FILTER (LPF) AND AGC

The baseband block contains a programmable gain LPF and output buffer. The 6th order BB LPF's cutoff frequency supports CMMB (UHF band), DTMB, DVB-H, DVB-T, T-DMB, ATSC-M/H and ISDB-T (full-seg, 3-seg and 1-seg) modes and 6 dB to 60 dB programmable gain by 0.25 dB step size. To compensate the LPF cutoff frequency variation, the automatic tuning circuit is included. The BB AGC controls the final output amplitude.

## AUTOMATIC GAIN CONTROL (AGC)

The ADMTV803 LNA has a 4-step gain control with dynamic range of 39 dB.

- The RFPGA has a dynamic gain range of 36 dB, and the RFAGC register controls it. The register value is from 0x00 (minimum gain) to 0x5F (maximum gain). The RFAGC consists of an LNA and an RFPGA. The RFAGC dynamic range is 75 dB.
- Baseband gain is determined by the digital gain setting which can be read via the GVBB register.

With these two dynamic ranges (RFAGC = 75 dB and BBAGC = 54 dB), the ADMTV803 dynamic range is larger than 100 dB. For more information about the RFAGC and BBAGC, see the RFAGC Setting and BBAGC Setting sections.

The recommended output amplitude of the ADMTV803 is from 300 mV to 700 mV (peak-to-peak voltage at each I/Q output pin). At 500 mV amplitude, the ADMTV803 exhibits its best performance.

## RF POWER DETECTOR AND ADJACENT RECEIVED SIGNAL STRENGTH INDICATOR (ADJRSSI)

The take-over point (TOP) divides the operating range of the RFAGC and BBAGC. The BBAGC voltage from the demodulator controls the GVBB. The demodulator generates the BBAGC voltage by measuring I and Q signal level of the tuner output. When the RF input level is getting lower than the TOP, demodulator increases BBPGA gain by increasing BBAGC voltage.

When the RF input level is higher than the TOP, the RFPGA operates. As the RF input level increases, RFPGA gain decreases. RF input level of the opposite direction makes RFPGA gain increased. In the middle of the RFPGA operation range, the LNA on/off operation occurs, and this operation expands the dynamic range of the RFAGC block.

## I²C INTERFACE AND CLOCK CONTROL

The ADMTV803 uses the I²C bus interface. The serial data (SDA) and serial clock (SCL) carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a master or slave, depending on the function of the device.

## POWER-DOWN MODES

The ADMTV803 has two power-down modes.

### *Software Power-Down*

The ADMTV803 has a software power-down mode controlled by the SWPD registers (Address 0x2F, Address 0x30 and Address 0x31).

### *Time-Slicing Power-Down*

The ADMTV803 also supports a time-slicing power-down mode. TSPD controls time-slicing power-down according to register setting (Address 0x31, Address 0x32 and Address 0x33). During time-slicing power down mode, each block can be selected to be on or off according to the register setting.

# APPLICATIONS INFORMATION

**Single(UHF) and Dual(VHF, UHF) Band Application**

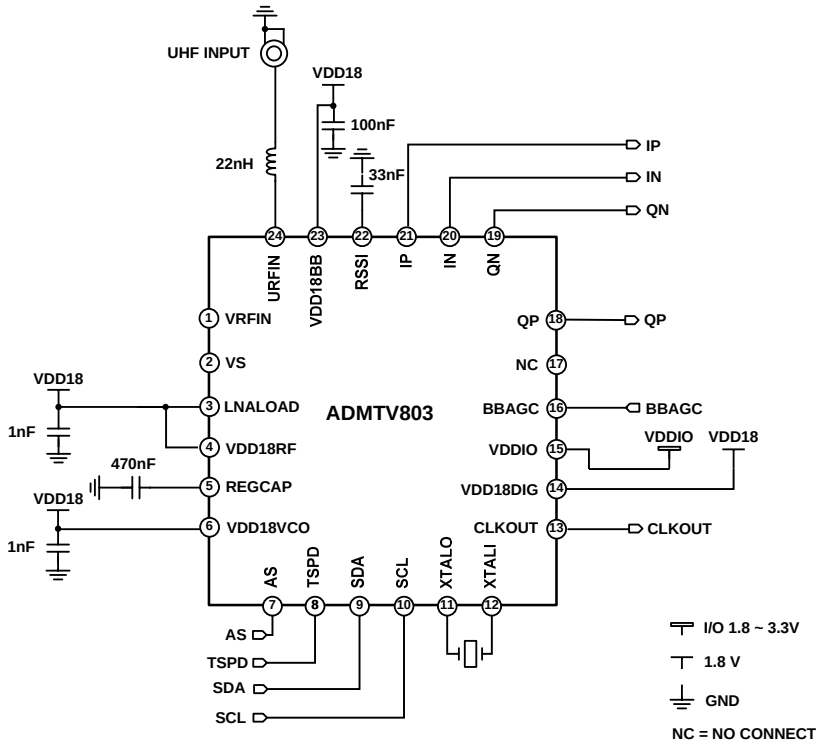



*Figure 31. Typical Application Circuit for UHF Single band*

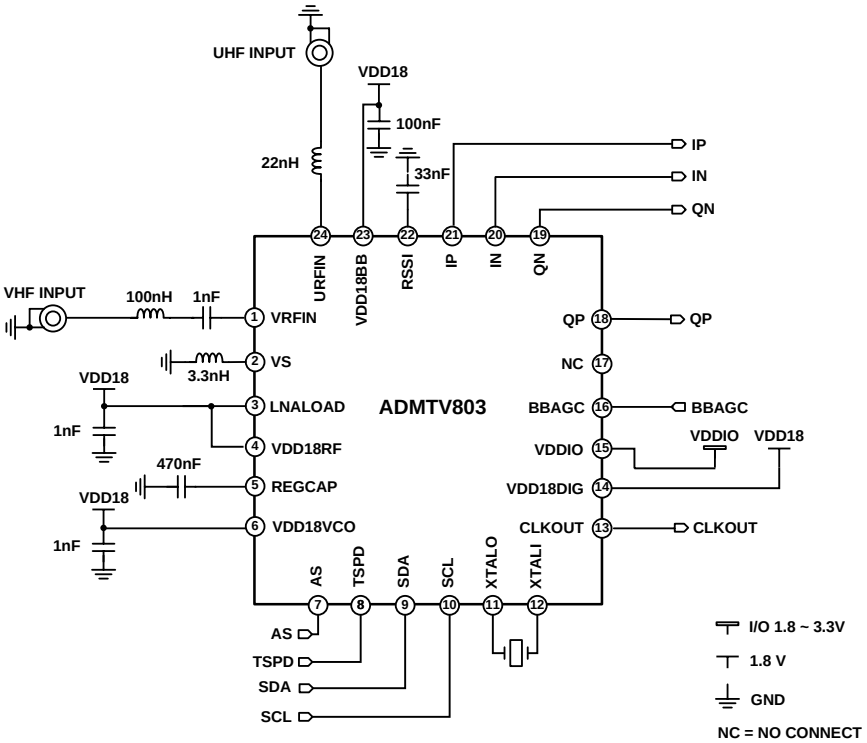
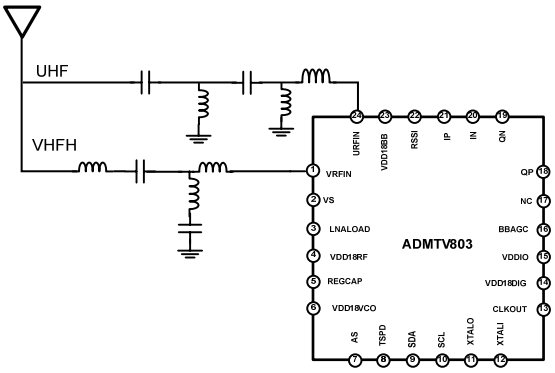
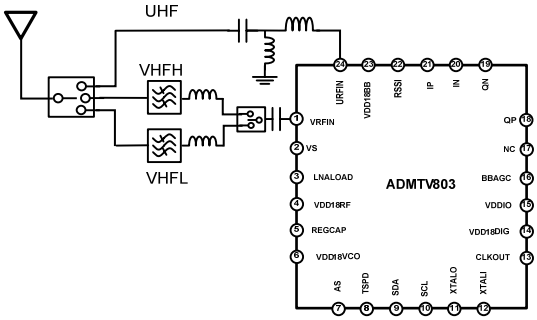



*Figure 32. Typical Application Circuit for Dual band*

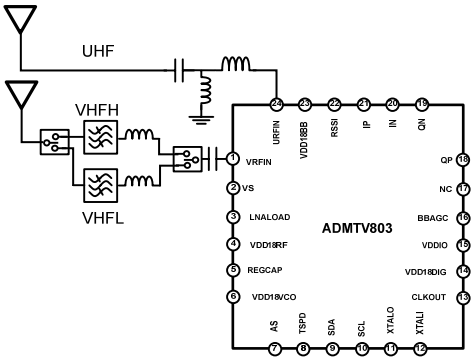
## ANTENNA APPLICATION INFORMATION



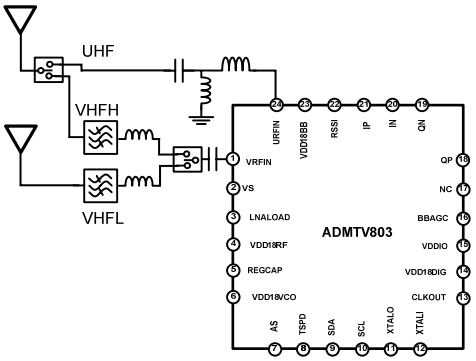

**I) One antenna solution for VHFH and UHF band**




**II) One antenna solution for VHFL, VHFH and UHF band**




**III) Two antennas solution for VHFL, VHFH and UHF band**




**IV) Two antennas solution for UHF, VHFH and VHFL band**

*Figure 33. Antenna Application Information*

## RF INPUT STAGE

The ADMTV803 requires RF impedance matching application circuit. The RF impedance matching components should be located as close as possible to the chip(see Figure 36). The VRFIN pin requires 1 nF DC-blocking capacitor to protect the DC coupling. RF impedance matching values can be changed to optimize RF performance. At UHFIN pin, a DC-blocking capacitor is integrated in the IC.

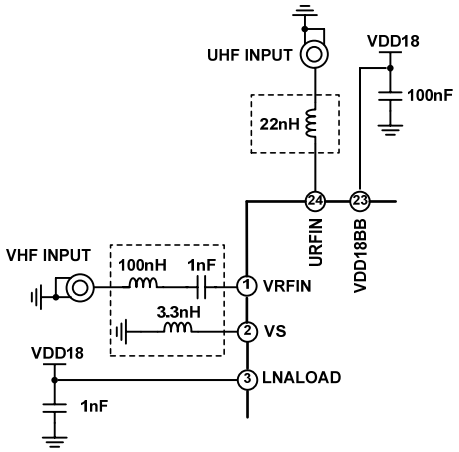



*Figure 34. RF Input Stage*

## VCO BIAS/BYPASS CAPACITORS

The ADMTV803 has integrated VCOs/PLLs for LO frequency generation. By using bypass capacitors, these VDD18 power lines should be isolated from noisy power sources. The bypass capacitor of VDD18 power rejects high frequency noise in the power supply. These bypass capacitors should be located as close as possible to chip and GND (see Figure 37).

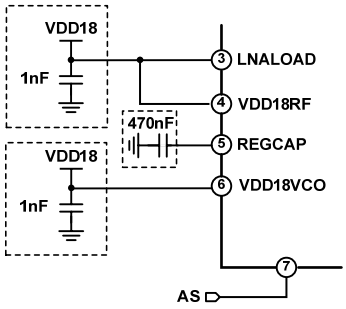



*Figure 35. VCO Bias/Bypass Capacitors*

## DIGITAL INTERFACE— SDA/SCL

The ADMTV803 is controlled by the I²C communication protocol. The serial data (SDA) and serial clock (SCL) carry information between the devices connected with the bus interface. SDA and SCL facilitate bidirectional communication between the ADMTV803 and the master at clock frequency up to 400 kHz. In addition, 10 kΩ pull-up resistors are integrated on chip for the demodulator interface (see Figure38).

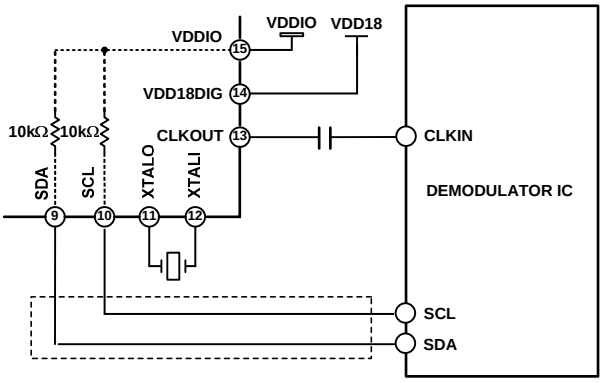



*Figure36. I²C Interface*

## BBAGC INTERCONNECTIONS

The ADMTV803 supports three AGC modes; analog mode, analog PWM mode and digital PWM mode. Each mode is controlled by demodulator's AGC signal which contains gain control information and it can be connected between demodulator's AGC and ADMTV803's BBAGC without external components (see Figure 39).

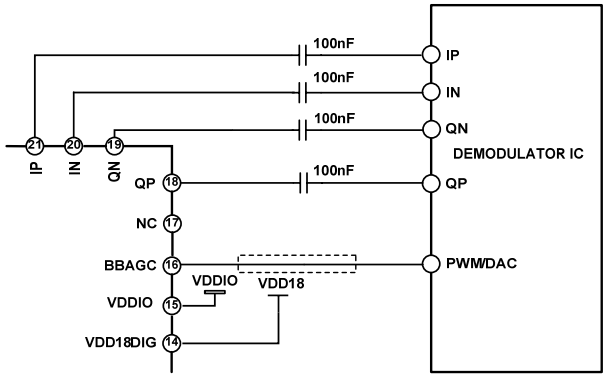



*Figure 37. AGC Connection*

Usually demodulator has AGC block which result is expressed as 1-bit PWM type signal. However, some demodulators feed D/A converted analog signal. Most of these feedback signals are accomplished by open-collector or open-drain scheme. ADMTV803 can accompany with any type of demodulator using PCB line connection that just enough by changing its own register setting. In the case of demodulator feedback signal is PWM signal type, the ADMTV803 has pull-up resistor and internal low-pass filtering block to handle PWM feedback signal by direct connection to demodulator. According to demodulator, a PWM signal is various. For these reasons, the ADMTV803 has two PWM signal processing methods, which are digital PWM and analog PWM mode.

Thus, the ADMTV803 supports every PWM output signal type of demodulator without external components.

1. Digital PWM mode

The ADMTV803 has a digital moving average filter. This filter can find the wanted gain control value of baseband. This mode does not require additional blocks between demodulator and ADMTV803. 1-bit PWM signal can be directly filtered out by tuning averaged data number of digital filter.

2. Analog PWM mode

Digital moving average filter only PWM signal processing may suffer from noise issues even though tuning number of averaged data. Therefore, the ADMTV803 also has internal analog low-pass filter for improving wanted baseband gain control value quality. The analog PWM mode employs cascaded analog low-pass filter and digital moving average filter. In this case, internal 8-bit A/D converter is used between analog low-pass filter and digital filter on chip.

3. Analog mode

In the other case of demodulator feedback signal is Analog mode (D/A converted analog signal), by using pull-up resistor and analog buffer, the ADMTV803 can find wanted BB gain control value in case of analog type feedback signal processing. This mode does not use digital moving average filter, but analog low-pass filter and A/D converter. The mode changing is accomplished easily by register tuning.

## XIN/XOUT INTERCONNECTIONS

The ADMTV803 supports crystal and temperature-controlled crystal oscillator (TCXO) for a reference clock. When using a crystal, XTALI and XTALO pins are connected to crystal unit. A 1 MΩ feedback resistor and 8 pF load capacitors are integrated on chip. (see Figure 40).

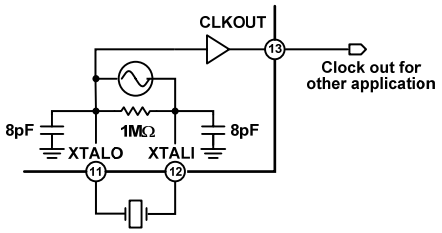



*Figure 38. X-TAL Application*

It is highly recommended to inquire an optimized oscillator application from crystal vendors.

The stability also depends on the demodulator's carrier tracking performance.

| Target Frequency (MHz) | 13 ~ 40 |
|---|---|
| Load Capacitor (pF) on chip | 8 |
| Maximum ESR (ohm) | TBD |
| Temperature Stability (ppm) | ± 30 |

In addition, the default setting of CLKOUT port at power-on state is the crystal frequency divided by 1. For example, if the crystal frequency is 30.4 MHz, then clock output frequency is 30.4 MHz when the chip starts after just power-on state. In case of using a temperature-controlled crystal oscillator (TCXO), it should be interfaced to the ADMTV803 via Pin XTALI with a DC block capacitor of 10 nF.

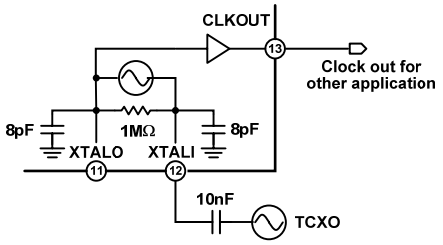



*Figure 39. TCXO Application*

It is also highly recommended to inquire an optimized oscillator application from TCXO vendors. TCXO output amplitude must be larger than 500 mV p-p. The stability also depends on the demodulator's carrier tracking performance.

| Target Frequency (MHz) | 13 ~ 40 |
|---|---|
| Load Capacitor (pF) on chip | 8 |
| Maximum ESR (ohm) | TBD |
| Temperature Stability (ppm) | ± 5 |

It is also noted that default frequency of CLKOUT port at power-on state is the TCXO frequency divided by 1. For example, if the TCXO frequency is 30.4 MHz, then clock output frequency is 30.4 MHz when the chip starts after just power-on state.

## REFERENCE CLOCK SELECTION

ADMTV803 supports reference clocks as below. Table 7 shows PLLR register selection.

**Table 6. PLLR selection according to crystal oscillator**

| Crystal oscillator | PLLR<3:0> |
|---|---|
| 13 MHz to 22 MHz | 0x01 |
| 23 MHz to 40 MHz | 0x02 |

## PLL SETTING

As stated in the Local Oscillator section, the ADMTV803 local oscillator (LO) consists of a VCO and a Σ-Δ fractional-N PLL. The ADMTV803 supports a wide range of LO frequencies as shown in Table 7. when using 30.4 MHz reference clock. When changing LO frequencies, users must calculate the PLLN and PLLF register values manually. The Manual PLL Setting Procedure section outlines the steps to adjust these two registers.

**Table 7. Register Value Selection[1]**

| VCOBAND<1:0>: VCO core frequency shift | | | | |
|---|---|---|---|---|
| VCOLOADBAND<1:0>: band selection | | | | |
| **LO Frequency** | **VCOBAND <1:0>** | **VCOLOADBAND <1:0>** | **PLLS (Dec)** | **PLLR <3:0>** |
| 54 MHz to 57 MHz | 0x3 | 0x0 | 8 | b10 |
| 58 MHz to 75 MHz | 0x0 | 0x0 | 8 | b10 |
| 75 MHz to 117MHz | 0x3 | 0x0 | 8 | b01 |
| 117 MHz to 150MHz | 0x0 | 0x1 | 4 | b10 |
| 150 MHz to 235 MHz | 0x3 | 0x1 | 4 | b01 |

| | | | | |
|---|---|---|---|---|
| 235 MHz to 300 MHz | 0x0 | 0x2 | 2 | b10 |
| 300 MHz to 470 MHz | 0x3 | 0x2 | 2 | b01 |
| 470 MHz to 600 MHz | 0x0 | 0x3 | 1 | b10 |
| 600 MHz to 940 MHz | 0x3 | 0x3 | 1 | b01 |

[1] The LO frequency is calculated by dividing the PLL frequency by the division ratio according to the PLLS

### *Manual PLL Setting Procedure*

To set the $f_{LO}$ manually, use the following procedure:

1. Reset the tuner.
2. Select the $f_{LO}$ to be oscillated.
3. Select the VCOBAND<1:0> register value and VCOLOADBAND<1:0> register value according to the $f_{LO}$ selection in Table 7.
4. The PLLS value is a division step decided by VCOLOADBAND<1:0> value selection.
5. Use the PLLR value, which has a default of 2 if you use 30.4MHz reference clock.
6. Determine the PLLN and PLLF register values by calculating the following equations:

$$f_{PLL} = \frac{f_{crytal}}{PLLR} \cdot \left( PLLN + \frac{PLLF}{2^{20}} \right)$$

$$f_{LO} = \frac{f_{PLL}}{PLLS}$$

where:

*PLLN* is the integer divide value selected by the PLLN register.
*PLLF* is the fractional divide value selected by the PLLF register.

*PLLR* is the reference crystal frequency divide ratio selected by PLLR register.
*PLLS* is selected by the VCOLOADBAND<1:0> register value and VCOBAND<1:0> register and frequency range decides VCOLOADBAND<1:0> register value. Solving these equations give one equation consisting of the PLLN and PLLF variables. PLLN is an integer value, and PLLF is a fractional value multiplied by $2^{20}$. For example, if the desired $f_{LO}$ = 666 MHz and crystal oscillator frequency = 30.4 MHz.

$$f_{PLL} = 30.4\,\text{MHz} \times \left( \text{PLLN} + \left( \frac{\text{PLLF}}{2^{20}} \right) \right)$$

$$f_{LO} = 666\ \text{MHz} = \frac{f_{PLL}}{PLLS} = \frac{f_{PLL}}{1}$$

$$666\ \text{MHz} = 30.4\,\text{MHz} \times \left( \text{PLLN} + \left( \frac{\text{PLLF}}{2^{20}} \right) \right)$$

$$\frac{666}{30.4} = \left( PLLN + \left( \frac{PLLF}{2^{20}} \right) \right)$$

$$43.81578947 = PLLN + \frac{PLLF}{2^{20}}$$

The PLLN and PLLF values are as follows:

$PLLN = 21 \rightarrow PLLN = 0x15$

$PLLF = 0.907894 \times 2^{20} = 991995 \rightarrow PLLF = 0xE86BB$

## RFAGC SETTING

The ADMTV803 has dual RF/BB AGC loops. The RF AGC and the BB AGC loops are controlled by demodulator. RF power detector and ADJ RSSI operate automatically to improve linearity for strong signals and interferer injection. RF and baseband PGA block gain can also be set manually for test purposes.

### *RF Gain Setting (Automatic and Manual Gain Control)*

The ADMTV803 RFAGC has two gain control mode, automatic gain control and manual gain control. When RFAGCSEL<1:0> is 0x0, (This is a default setting) RFAGC operates as automatic control mode. For flexibility of RF gain control, the LNA could be controlled independently by changing RFAGCSEL<1:0>.

| RFAGCSEL <1:0> | Description |
|---|---|
| 0x0 | Fully automatic RF gain control |
| 0x1 | Automatic gain control of LNA, Manual control of remained RF blocks |
| 0x2 | Manual control of LNA gain, Automatic gain control of remained RF blocks |
| 0x3 | Fully manual RF gain control |

LNAGAIN_I2C<1:0> and RFAGC_I2C<6:0> could be written LNA gain and RFPGA block gain respectively. These manually set gains will be asserted according to the RFAGC<1:0>.

## BB GAIN SETTING

For automatic gain control of BB PGA, the ADMTV803 supports three BBAGC mode, which are digital PWM mode, analog PWM mode and analog mode. Furthermore, the ADMTV803 can set BB PGA gain via manual gain control register setting.

### *Automatic BB Gain Setting*

At initial setting, BB gain(GVBB) is under analog PWM mode. To utilize the BBAGC demodulator feedback signal at this mode,

1. Set GVBBSEL<0> to 0x0
2. Connect the demodulator feedback of BBAGC to the ADMTV803 directly (Pin 16)

Digital PWM mode is enabled by changing BBAGCMODE_SEL<0> as '1'. There is no difference of PCB

connection as changing PWM mode from analog PWM to digital PWM mode. The ADMTV803 has internal pull-up resistors to remove external components for demodulator's open-collector or open-drain output. In this case,

1. Set GVBBSEL<0> to 0x0
2. Set R_BBAGC_PU<2:0> to the desired value. (Refer the I2C map table in detail)
3. Connect the BBAGC of demodulator feedback to the ADMTV803 directly (Pin 16)

On the other hand, analog mode requires different register settings as follows.

1. Set GVBBSEL<0> to 0x0
2. Set SEL_BBAGCIN_AMODE<0> to 0x1 (Default setting is 0x0)
3. Connect the BBAGC of demodulator feedback to the ADMTV803 directly. (Pin 16)

Same pull-up resistors, R_BBAGC_PU<2:0> can be set according to the demodulator conditions which are digital and analog PWM mode type.

### *Manual Gain Setting*

For manual gain setting, gain control mode must change to manual gain setting. When GVBBSEL<0> set to '1' then BB gain control goes to manual mode. Then, BB gain is controlled by changing GVBB_I2C<7:0>.

1. Set GVBBSEL<0> to 0x1
2. Set GVBB_I2C<7:0> to the desired value (0x00 to 0xD7)

## TSPD CONTROL SIGNAL INVERTING

The ADMTV803 time-slicing power-down (TSPD) polarity can be inverted by users demand.

| TSPDPOL<0> | Status |
|---|---|
| 0x0 | Normal |
| 0x1 | Inverse |

## POWER-DOWN CONTROL

The ADMTV803 has two power-down modes: time-slicing power-down (TSPD pin), and software power-down (SWPD register settings). Recovery time from power-down depends on the PLL lock time and the demodulator's AGC response.

- If the TSPD pin is high and a TSPDxxx block register (Address 0x31, Address 0x32 and Address 0x33) is high, the xxx block is powered down.
- If a SWPDxxx block register is high, the xxx block register (Address 0x2F, Address 0x30 and Address 0x31) is powered down.

In case of time-slicing power-down, all blocks including the crystal oscillator block are powered down. Therefore, all digital parameters are stored as they were before power-down.

After being powered on by the TSPD pin, the tuner does not need to operate the VCO searching loop and automatic gain control.

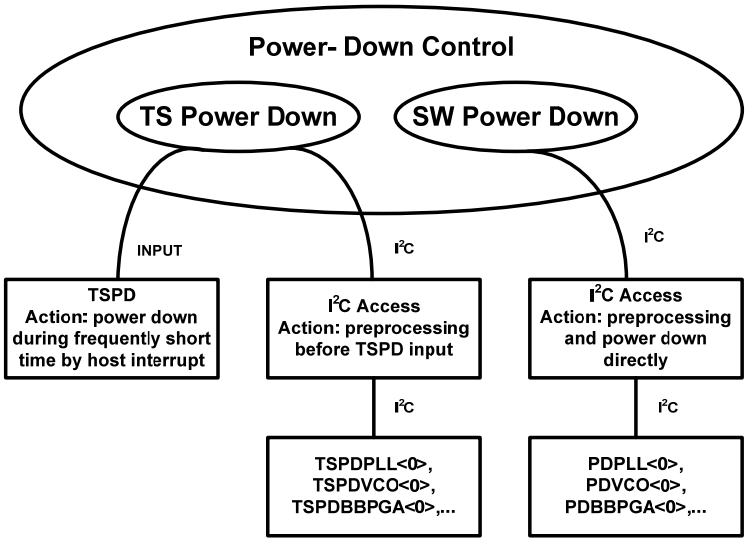



*Figure 40. Two Power-Down Modes*

# I²C OPERATION

The ADMTV803 is controlled by an I²C data bus and is compatible with both standard and fast mode formats. The data and clock are fed on the SDA and SCL lines, respectively, as defined by the I²C bus format. The device can either accept data in the write-mode, or send data in the read-mode. The LSB of the address byte sets the device into write-mode if it is low and read mode if it is high.

## I²C READ/WRITE ADDRESS

**Table 8. I²C Read Address**

| Address Select Pin (AS) | MSB | | | | | | | LSB | Address (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| Low | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0xC3 |
| High | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0xC5 |

**Table 9. I²C Write Address**

| Address Select Pin (AS) | MSB | | | | | | | LSB | Address (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| Low | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0xC2 |
| High | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0xC4 |

## I²C BUS FORMAT

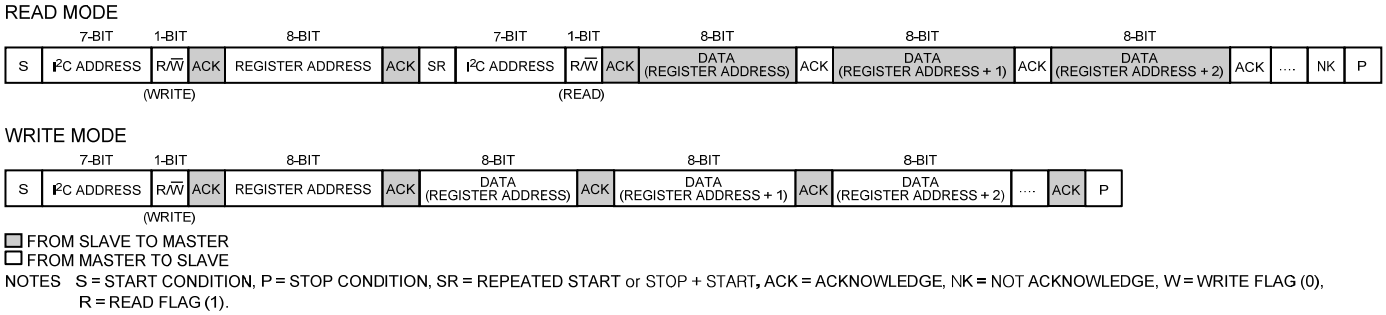
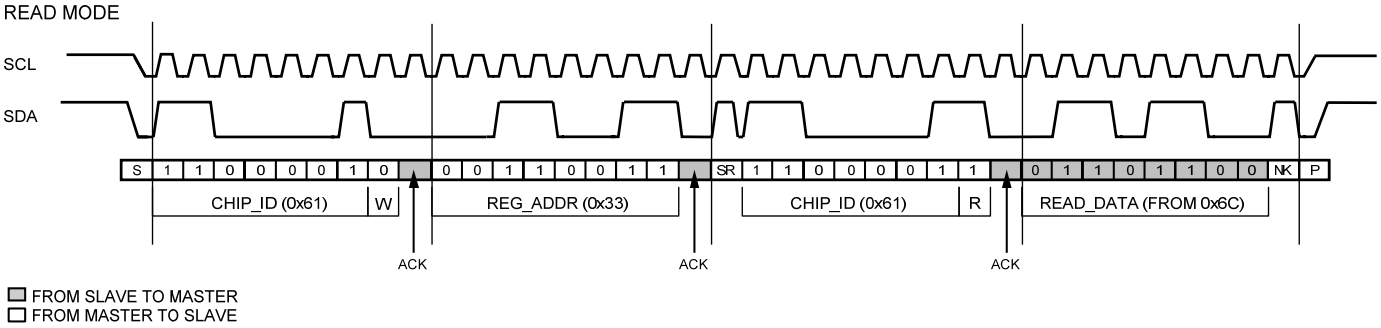



Figure 41. I²C Bus Format

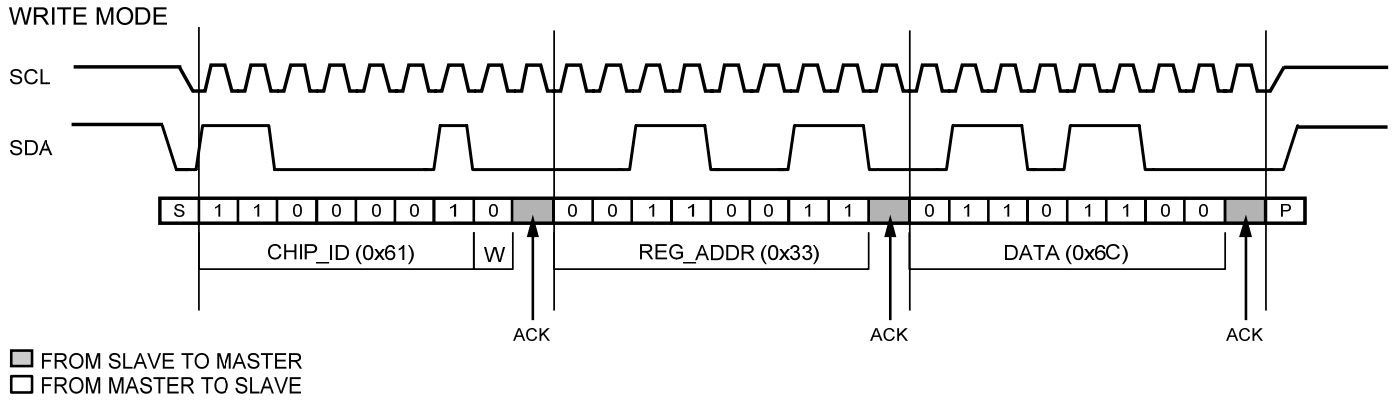
## I²C TIMING CHARACTERISTICS

According to standard I²C specification, the clock frequency reaches its maximum 400 kHz in fast-mode and 100 kHz in standard-mode. To communicate with RF tuner, users need to comply with the conditions in this section.




NOTES
1. S = START CONDITION, P = STOP CONDITION, SR = REPEATED START CONDITION or STOP + START CONDITION
   ACK = ACKNOWLEDGE: ACTIVE LOW, NK = NOT ACKNOWLEDGE: ACTIVE HIGH, W = WRITE MODE, R = READ MODE.
2. ADMTV803 MEETS THE DEMANDING PERFORMANCE SPECIFICATION OF I²C COMBINED MODE. THEREFORE, UPPER ACCESS CONDITION IS ABLE TO BE MODIFIED ON STANDARD I²C.

*Figure 42. Serial Control Port Read Mode*




NOTES
1. S = START CONDITION, P = STOP CONDITION, ACK = ACKNOWLEDGE: ACTIVE LOW, W = WRITE MODE, R = READ MODE,
2. ADMTV803 MEETS THE DEMANDING PERFORMANCE SPECIFICATION OF I²C COMBINED MODE. THEREFORE, UPPER ACCESS CONDITION IS ABLE TO BE MODIFIED ON STANDARD I²C.

*Figure 43. Serial Control Port Write Mode*

### *Serial Control Port Timing*

$T_A$ = 25°C, $V_{DDIO}$ = 2.8 V, GND = 0 V, unless otherwise noted.

**Table 10. I²C Serial Control Timing**

| Parameter | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Hold Time (Repeat) Start Condition[1] | $t_{SHD}$ | 4.0 | | 0.6 | | µs |
| SCL Clock Period | $t_{CLK}$ | 0 | 100 | 0 | 400 | kHz |
| High Period of the SCL Clock | $t_{HIGH}$ | 4.0 | | 0.6 | | µs |
| Low Period of the SCL Clock | $t_{LOW}$ | 4.7 | | 1.3 | | µs |
| Setup Time for Stop Condition | $t_{PSU}$ | 4.0 | | 0.6 | | µs |
| Data Setup Time | $t_{DSU}$ | 250 | | 100[2] | | ns |
| Data Hold Time for I²C Bus Devices | $t_{DHD}$ | 0[3] | 3.45[4] | 0[3] | 0.9[4] | µs |

[1] After this period, the first clock pulse is generated.

[2] A fast mode I2C bus device can be used in a standard mode I2C bus system, but the $t_{DSU}$ ≥250ns requirement must then be met. This automatically occurs if the device does not stretch the low period of the SCL signal ($t_{LOW}$)

[3] A device must internally provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

[4] The maximum $t_{DHD}$ needs to be met only when the device does not stretch the low period of the SCL signal ($t_{LOW}$)

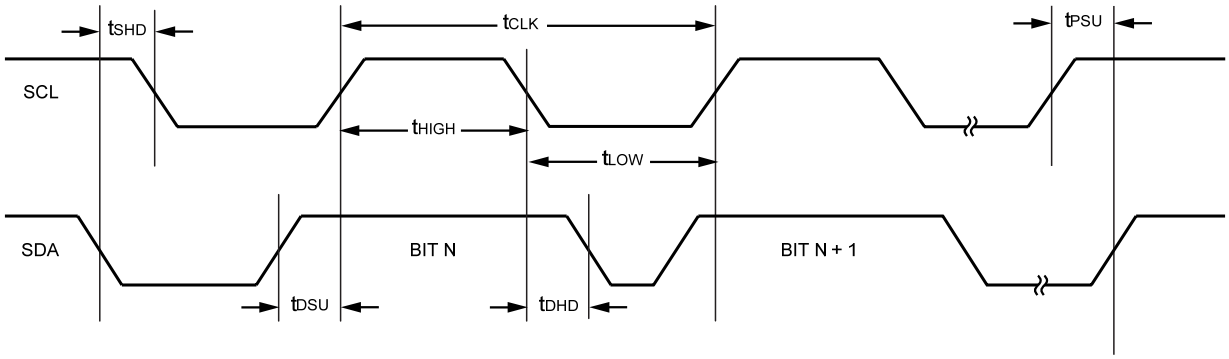



*Figure 44. Serial Control Port Timing*

## I²C REGISTER MAP

**Table 11. Register Listing**

| Addr (Hex) | Type | Parameter | (MSB) Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | (LSB) Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | R | CHIPID | CHIPID1<7:0> | | | | | | | |
| 0x01 | R | CHIPID0 | CHIPID0<7:0> | | | | | | | |
| 0x02 | R | SPLITID | SPLITID<7:0> | | | | | | | |
| 0x03 | R | RFAGC | BLANK | RFAGC<6:0> | | | | | | |
| 0x04 | R | BBAGC | GVBB<7:0> | | | | | | | |
| 0x05 | R | RFAGC /LNA | BLANK | | | | CH_FLAG_OUT<1:0> | | LNAGAIN<1:0> | |
| 0x07 | R | VCO/PLL | BLANK | RESERVED | | | | | LOCK | |
| 0x08 | R | ADC | BLANK | RV<5:0> | | | | | CTUNE<8> | |
| 0x09 | R | CTUNE | CTUNE<7:0> | | | | | | | |
| 0x12 | R | EFUSE | BLANK | | | READEFUSE<12:8> | | | | |
| 0x13 | R | EFUSE | READEFUSE<7:0> | | | | | | | |
| 0x22 | R/W | LNA | LNABAND | RESERVED | | | | | | |
| 0x23 | R/W | LNA | ICONLNA_NORM<3:0> | | | | ICONLNA_SENS<3:0> | | | |
| 0x24 | R/W | LNA/LPF | ICONLNA_ACR<3:0> | | | | MODE1: CMMB 8M DVB-T/H, ISDB-T FULL SEG, ATSC (TBD) | MODE2: CMMB 2M | MODE3: T-DMB, ISDB-T 1SEG ISDB-T 3SEG | RESERVED |
| 0x25 | R/W | LNA/LPF | PDDIV3 | PDUHF | PDVHFH | PDVHFM | PDVHFL | RESERVED | | |
| 0x26 | R/W | VCO/PLL | VCOLOADBAND<1:0> | | RESERVED | | VCOBAND<1:0> | | PLLN<9:8> | |
| 0x27 | R/W | PLL | PLLN<7:0> | | | | | | | |
| 0x28 | R/W | PLL | PLLF<19:12> | | | | | | | |
| 0x29 | R/W | PLL | PLLF<11:4> | | | | | | | |
| 0x2A | R/W | PLL | PLLF<3:0> | | | | PLLR<3:0> | | | |
| 0x2B | R/W | PLL/BBAGC | BLANK | RST_PLL | INIT_VCOCAL | RESERVED | SEL_BBAGCIN_AMODE | R_BBAGC_PU<2:0> | | |
| 0x2E | R/W | BBAGC | BLANK | BBAGC MODE_SEL | POL_BBAGC | ADC_BP_SEL | AVGCNT_SET<3:0> | | | |
| 0x2F | R/W | SWPD | SWPDLNA | SWPDMIX | SWPDBB | SWPDVCO | SWPDLDO | SWPDPLL | SWPDBGR | SWPDPDET |
| 0x30 | R/W | SWPD | SWPD ADJRSSI | SWPDADC | SWPDBBAGC ANALOG | SWPDDCOSDAC | SWPD CTUNE | SWPDRTUNE | SWPD TMPSNS | SWPDDIG |
| 0x31 | R/W | SWPD/TSPD | SWPDCLKDRV | SWPDOSC | TSPDLNA | TSPDMIX | TSPDBB | TSPDVCO | TSPDLDO | TSPDPLL |
| 0x32 | R/W | TSPD | TSPDBGR | TSPDPPDET | TSPDADJRSSI | TSPDADC | TSPDBBAGC ANALOG | TSPDDCOSDAC | TSPDC TUNE | TSPDRTUNE |
| 0x33 | R/W | TSPD/DIVIDER CLOCK OUTPUT | BLANK | | TSPDTMPSNS | TSPDDIG | TSPDCLKDRV | TSPDOSC | DIVCLKDRV<1:0> | |
| 0x3C | R/W | MIXER/LNA | BLANK | MIXSELBGR | RESERVED | | MIXGAIN BOOST | RESERVED | | |
| 0x3D | R/W | MIXER/PWR. DETECTOR | CALPWD | RESERVED | | | MIXCTUNE<3:0> | | | |
| 0x3E | R/W | LPF | BLANK | RESERVED | STG2_Q_CAL<2:0> | | | STG3_Q_CAL<2:0> | | |
| 0x4B | R/W | LPF | BQC<7:0> | | | | | | | |
| 0x4D | R/W | RFAGC/VCO | DETENA | RESERVED | | | ADJENA | RESERVED | | |
| 0x4E | R/W | TSPD/VCO | TSPDPOL | RESERVED | | | PDPTATDIV | RESERVED | | |
| 0x59 | R/W | RESERVED | ENRTUNE | RESERVED | | | | | | |

| Addr (Hex) | Type | Parameter | (MSB) Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | (LSB) Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x5D | R/W | BBAGC | GVBBSEL | RESERVED | | | | | | |
| 0x7F | R/W | LNA | LNAGAIN_I2C<1:0> | | RESERVED | | | | | |
| 0x80 | R/W | RFAGC | RFAGCSEL<1:0> | | RESERVED | | | | | |
| 0x88 | R/W | BBAGC | IGCAL<3:0> | | | | QGCAL<3:0> | | | |
| 0x89 | R/W | RFAGC | BLANK | RFAGC_I2C<6:0> | | | | | | |
| 0x8B | R/W | PWR. DETECTOR | BLANK | PWD_DCOSDAC<5:0> | | | | | | |
| 0x93 | R/W | MIXER | RESERVED | | | | MIXICAL<1:0> | | MIXQCAL<1:0> | |

NOTES

The RESERVED bits are not supposed to be changed.

R: Read only.

R/W: Read and Write.

## REGISTER DESCRIPTIONS

**Table 12. Read Only Register**

| Address (Hex) | Bit(s) | Name | Description |
|---|---|---|---|
| 0x00 | <7:0> | CHIPID1<7:0> | Chip ID. |
| 0x01 | <7:0> | CHIPID0<7:0> | Chip ID. |
| 0x02 | <7:0> | SPLITID<7:0> | Chip split ID. |
| 0x03 | <6:0> | RFAGC<6:0> | RFAGC gain state value. |
| 0x04 | <7:0> | GVBB<7:0> | BBAGC gain control (0.25dB Step).<br><7:0> = 0x00: minimum gain.<br><7:0> = 0xD7: maximum gain. |
| 0x05 | <3:2> | CH_FLAG_OUT<1:0> | Channel state flag output.<br><1:0> = 0x0: normal state.<br><1:0> = 0x1: sensitivity state.<br><1:0> = 0x2: ACR state. |
| | <1:0> | LNAGAIN<1:0> | LNA gain state.<br><1:0> = 0x0: very low gain.<br><1:0> = 0x1: low gain.<br><1:0> = 0x2: middle gain.<br><1:0> = 0x3: high gain. |
| 0x07 | <0> | LOCK<0> | PLL lock indicator.<br><0> = 0x0: PLL is unlocked.<br><0> = 0x1: PLL is locked. |
| 0x08 | <6:1><br><0> | RV<5:0><br>CTUNE<8> | Internal RTUNE setting value.<br>Calculated C TUNE setting value. |
| 0x09 | <7:0> | CTUNE<7:0> | Calculated C TUNE setting value. |
| 0x12 | <4:0> | READEFUSE<12:8> | Read Fuse programming data in READ mode |
| 0x13 | <7:0> | READEFUSE<7:0> | Read Fuse programming data in READ mode |

**Table 13. Read/Write Register**

| Address (Hex) | Bit(s) | Name | Description |
|---|---|---|---|
| | | | LNA/MIXER |
| 0x22 | <7> | LNABAND<0> | LNA band selection.<br><0> = 0x0: VHF<br><0> = 0x1: UHF |
| 0x3C | <6> | MIXSELBGR<0> | Mixer Bias current selection.<br><0> = 0x0: PTAT current<br><0> = 0x1: BGR current |

| | | | |
|---|---|---|---|
| | <3> | MIXGAINBOOST<0> | Mixer Gain manual control.<br><0> = 0x0: default<br><0> = 0x1: 6dB gain increase |
| 0x3D | <3:0> | MIXCTUNE<3:0> | Mixer trans-impedance amplifier 1st order low pass filter capacitor tuning control.<br><3:0> = 0x0: BW maximum<br><3:0> = 0xF: BW minimum |
| 0x93 | <1:0> | MIXQCAL<1:0> | Mixer's phase calibration<br><1:0> = 0x0: 0 degree<br><1:0> = 0x3: -3 degree |
| | <3:2> | MIXICAL<3:2> | Mixer's phase calibration<br><1:0> = 0x0: 0 degree<br><1:0> = 0x3: +3 degree |
| | | BASEBAND | |
| 0x24 | <3> | MODE1<0>: CMMB 8M DVB-T/H, ISDB-T FULL SEG, ATSC-M/H | LPF cutoff frequency selection.<br><0> = 0x1: Mode1 (MODE2<0> and MODE3<0> = 0x0). |
| | <2> | MODE2<0> : CMMB 2M | LPF cutoff frequency selection.<br><0> = 0x1: MODE2 (MODE1<0> and MODE3<0> = 0x0). |
| | <1> | MODE3<0> : T-DMB, ISDB-T 1SEG, ISDB-T 3SEG | LPF cutoff frequency selection<br><0> = 0x1: MODE3 (MODE1<0> and MODE2<0>= 0x0). |
| 0x3E | <5:3> | STG2_Q_CAL<2:0> | Biquad LPF 2nd stage Q control. |
| | <2:0> | STG3_Q_CAL<2:0> | Biquad LPF 3rd stage Q control. |
| 0x4B | <7:0> | BQC<7:0> | Cap. bank value after Fc tuning. This value can be changed by Fc tuning |
| | | VCO/PLL | |
| 0x25 | <7> | PDDIV3<0> | Power down div3 path. |
| | <6> | PDUHF<0> | Power down UHF path. |
| | <5> | PDVHFH<0> | Power down VHF high path. |
| | <4> | PDVHFM<0> | Power down VHF middle path. |
| | <3> | PDVHFL<0> | Power down VHF low path. |
| 0x26 | <7:6> | VCOLOADBAND<1:0> | Select of band.<br><1:0> = 0x0 : VHFL<br><1:0> = 0x1 : VHFM<br><1:0> = 0x2 : VHFH<br><1:0> = 0x3 : UHF |
| | <3:2> | VCOBAND<1:0> | VCO core frequency range selection (manual control.<br><1:0>= 0x0: low freq<br><1:0>= 0x3: high freq |
| | <1:0> | PLLN<9:8> | PLL feedback divider integer words. |
| 0x27 | <7:0> | PLLN<7:0> | PLL feedback divider integer words. |
| 0x28 | <7:0> | PLLF<19:12> | PLL feedback divider fractional words. |
| 0x29 | <7:0> | PLLF<11:4> | PLL feedback divider fractional words. |
| 0x2A | <7:4> | PLLF<3:0> | PLL feedback divider fractional words. |
| | <3:0> | PLLR<3:0> | PLL reference divider integer value. |
| 0x2B | <6> | RST_PLL<0> | PLL reset.<br><0>= 0x1: Reset<br><0>= 0x0 : Release |
| | <5> | INIT_VCOCAL<0> | Initial VCO search loop start reset signal.<br><0>= 0x0 ->0x1 |
| | | RF POWER DETECTOR | |
| 0x3D | <7> | CALPWD<0> | Power Detector DC Offset Calibration mode.<br><0> = 0x0: stop calibration<br><0>= 0x1: calibration |
| 0x8B | <5:0> | PWD_DCOSDAC<5:0> | 6-bit input of Power Detector DC offset Calibration DAC. |

| | | | |
|---|---|---|---|
| BBAGC INTERFACE | | | |
| 0x2B | <3> | SEL_BBAGCIN_AMODE<0> | AGC input selection mode at ADC mode.<br><0>= 0x0 : PWM signal is connected to analog AGC LPF<br><0>= 0x1 : analog signal which is buffered by analog buffer is connected to analog AGC LPF. |
| | <2:0> | R_BBAGC_PU<2:0> | Pull up resistor value control.<br><2:0> = 0x0 : open<br><2:0> = 0x1 : 10 k Ohm<br><2:0> = 0x2 : 7.07 k Ohm<br><2:0> = 0x3 : 5 k Ohm<br><2:0> = 0x4 : 3.5 k Ohm<br><2:0> = 0x5 : 2.5 k Ohm<br><2:0> = 0x6 : 1.77 k Ohm<br><2:0> = 0x7 : 1.25 k Ohm |
| BBAGC | | | |
| 0x2E | <6> | BBAGCMODE_SEL<0> | Selection bit to determine the BBAGC mode.<br><0>=0x0: ADC mode<br><0>=0x1: PWM mode |
| | <5> | POL_BBAGC<0> | Polarity inverting bit of PWM input signal.<br><0>=0x0: Proportional PWM signal duty cycle.<br><0>=0x1: Inverse proportional PWM signal duty cycle |
| | <4> | ADC_BP_SEL<0> | Selection bit.<br><0>=0x0: Average filter output<br><0>= 0x1: Bypassing ADC input when '1' asserted. |
| | <3:0> | AVGCNT_SET<3:0> | To set the averaging date number of BBAGC average filter (Maximum value = 0xA)<br>Number of averaged data = 2^(AVGCNT_SET + 1 + 8 * BBAGCMODE_SEL) |
| 0x5D | <7> | GVBBSEL<0> | GVBB decoder selection bit.<br><0>=0x0: GVBB decoded output<br><0>=0x1: GVBB_I2C value |
| 0x87 | <7:0> | GVBB_I2C<7:0> | Manual setting value for GVBB |
| 0X88 | <3:0><br><7:4> | QGCAL<3:0><br>IGCAL<3:0> | BB Q path gain calibration value<br>BB I path gain calibration value |
| RTUNE | | | |
| 0x80 | <5:0> | RVI2C<5:0> | External rtune code input. if extrtune is high, RVI2C is bypassed to RV |
| EFUSE | | | |
| 0x2B | <4> | READEN | After chip reset, READEN should go to high (>10us) and then fall to low to make READEFUSE data valid |
| RF AGC | | | |
| 0x4D | <7> | DETENA<0> | Data enable bit to using A-to-D converted of RF power detector data for RFAGC internal calculation. |
| | <3> | ADJENA<0> | Data enable bit from ADJ RSSI. |
| 0x7F | <7:6> | LNAGAIN_I2C<1:0> | Manual control LNA gain value. |
| 0x80 | <7:6> | RFAGCSEL<1:0> | Selection bit.<br><1:0>=0x0: Calculated LNA gain code, Calculated RFAGC value<br><1:0>=0x1: Calculated LNA gain code, Manually asserted RFAGC value<br><1:0>=0x2: Manually asserted LNA gain code, Calculated RFAGC value<br><1:0>=0x3: Manually asserted LNA gain code, Manually asserted RFAGC value |
| 0x82 | <5:3> | SATSTEP<2:0> | AGC counter step at saturation mode = 2^(SATSTEP) |
| 0x89 | <6:0> | RFAGC_I2C<6:0> | Manual control RFAGC value. |
| CLOCK OUTPUT DRIVER | | | |
| 0x33 | <1:0> | DIVCLKDRV<1:0> | Divider for clock output driver.<br><1:0>=0x0: Output = master clock<br><1:0>=0x1: Output = master clock / 2<br><1:0>=0x2: Output = master clock / 4 |
| SOFTWARE POWER DOWN | | | |
| 0x2F | <7> | SWPDLNA<0> | Software power down of LNA. |

| | | | |
|---|---|---|---|
| | | | <0>=0x0: power on<br><0>=0x1: power down |
| | <6> | SWPDMIX<0> | Software power down of mixer.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <5> | SWPDBB<0> | Software power down of baseband.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <4> | SWPDVCO<0> | Software power down of VCO.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <3> | SWPDLDO<0> | Software power down of LDO.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <2> | SWPDPLL<0> | Software power down of PLL.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <1> | SWPDBGR<0> | Software power down of BGR.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <0> | SWPDPDET<0> | Software power down of RF power detector.<br><0>=0x0: power on<br><0>=0x1: power down |
| 0x30 | <7> | SWPDADJRSSI<0> | Software power down of ADJRSSI.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <6> | SWPDADC<0> | Software power down of ADC.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <5> | SWPDBBAGCANALOG<0> | Software power down of BBAGC analog part.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <4> | SWPDDCOSDAC<0> | Software power down of DC offset DAC.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <3> | SWPDCTUNE<0> | Software power down of CTUNE.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <2> | SWPDRTUNE<0> | Software power down of RTUNE.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <1> | SWPDTMPSNS<0> | Software power down of temperature sensor.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <0> | SWPDDIG<0> | Software power down of digital (clock gating).<br><0>=0x0: power on<br><0>=0x1: power down |
| 0x31 | <7> | SWPDCLKDRV | Software power down of clock driver.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <6> | SWPDOSC | Software power down of crystal oscillator.<br><0>=0x0: power on<br><0>=0x1: power down |
| | | | TIME-SLICING POWER DOWN |
| 0x31 | <5> | TSPDLNA<0> | Time-slicing power down of LNA. |

| | | | |
|---|---|---|---|
| | | | <0>=0x0: power on<br><0>=0x1: power down |
| | <4> | TSPDMIX<0> | Time-slicing power down of mixer.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <3> | TSPDBB<0> | Time-slicing power down of baseband.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <2> | TSPDVCO<0> | Time-slicing power down of VCO.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <1> | TSPDLDO<0> | Time-slicing power down of LDO.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <0> | TSPDPLL<0> | Time-slicing power down of PLL.<br><0>=0x0: power on<br><0>=0x1: power down |
| 0x32 | <7> | TSPDBGR<0> | Time-slicing power down of BGR.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <6> | TSPDPDET<0> | Time-slicing power down of RF power detector.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <5> | TSPDADJRSSI<0> | Time-slicing power down of ADJRSSI.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <4> | TSPDADC<0> | Time-slicing power down of ADC.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <3> | TSPDBBAGCANALOG<0> | Time-slicing power down of BBAGC analog part.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <2> | TSPDDCOSDAC<0> | Time-slicing power down of DC offset DAC.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <1> | TSPDCTUNE<0> | Time-slicing power down of CTUNE.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <0> | TSPDRTUNE<0> | Time-slicing power down of RTUNE.<br><0>=0x0: power on<br><0>=0x1: power down |
| 0x33 | <5> | TSPDTMPSNS<0> | Time-slicing power down of temperature sensor.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <4> | TSPDDIG<0> | Time-slicing power down of digital (clock gating).<br><0>=0x0: power on<br><0>=0x1: power down |
| | <3> | TSPDCLKDRV<0> | Time-slicing power down of clock driver.<br><0>=0x0: power on<br><0>=0x1: power down |
| | <2> | TSPDOSC<0> | Time-slicing power down of crystal oscillator.<br><0>=0x0: power on<br><0>=0x1: power down |
| 0x4E | <7> | TSPDPOL | TSPD polarity change.<br><0>=0x0: normal<br><0>=0x1: inverse |

NOTES

R: Read only.

R/W: Read and Write.

# OUTLINE DIMENSIONS

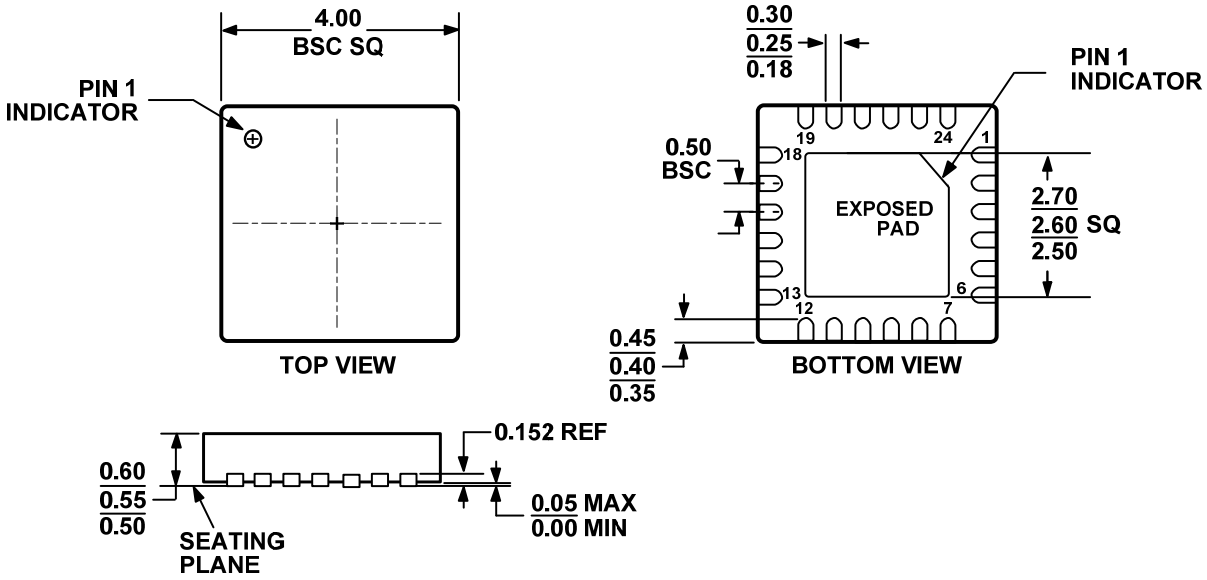



*Figure 45. 24-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm ×4 mm Body Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Band | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|
| ADMTV803ACPZRL[1] | UHF | −40°C to + 85°C | 24-Lead Frame Chip Scale Package [LFCSP] | CP-24-4 |
| ADMTV803BCPZRL[1] | UHF, VHF | −40°C to + 85°C | 24-Lead Frame Chip Scale Package [LFCSP] | CP-24-4 |
| ADMTV803A-EBZ[1] | UHF | | Evaluation Board | |
| ADMTV803B-EBZ[1] | UHF, VHF | | Evaluation Board | |

[1]Z = RoHS Compliant Part.

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